

Notice of References Cited	Application/Control No. 09/960,495	Applicant(s)/Patent Under Reexamination AMISHIRO ET AL.	
	Examiner Timothy J Sutton	Art Unit 2813	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2002/0033519	09-2001	Babcock et al.	257/536
	B	US-6,232,104	05-2001	Lishanski et al.	435/6
	C	US-5,135,882	08-1992	Karniewicz, Joseph J.	257/538
	D	US-6,130,139	10-2000	Ukeda et al.	438/353
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf, S., Silicon Processing for the VLSI ERA-Volume 2: Process Integration, 1990 by Lattice Press, Volume 2, pages 48-49.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.